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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,906	11/03/2003	Jason Harold Culler	200310793-1	4393
22879	7590	10/14/2005	EXAMINER	
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			NGUYEN, MINH T	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,906	CULLER, JASON HAROLD	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 12 September 2005.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-8, 10-12, 14-20, 23-28, 30 and 32-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 12, 14-20, 23-28, 30 and 34 is/are allowed.
- 6) Claim(s) 1, 5, 7, 8, 10, 11 and 32 is/are rejected.
- 7) Claim(s) 2-4, 6 and 33 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 03 November 2003 is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/12/05 has been entered.

Claim Objections

2. Claims 1-2 and 30 are objected to because of the following informalities:

In claim 1, line 7, "sampling system" should be changed to -- second sampling system -- to avoid potential antecedent basis problem, see line 4 of claim 2.

In claim 2, line 4, "a second sampling system" should be changed to -- the second sampling system --.

In claim 30, line 2, "internal clock signal" should be changed to -- internally generated signal -- for consistency, see line 4 of claim 24.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5, 7-8 and 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,701,445, issued to Majos.

As per claim 1, Majos discloses a system (figure 1), comprising:

an input that receives a synchronization signal having a frequency (the input node 1E which receives the input clock signal DIN); and
an oscillator/control system (the combination of circuit blocks 3, 4, 5 and VCO) that provides a clock signal having a frequency (the clock signal H which is output from the VCO), the oscillator/control system adjusts the clock signal based on a comparison the frequency for the synchronization signal and the frequency for the clock signal (the result from the frequency comparator 3 is fed to the control system (circuits 4 and 5) to adjust the clock signal H using the VCO), and

a sampling system (sampling circuit 1) that comprises a delay network (figure 2, the delay lines 11, 12 and 13) that provides plural output signals (Q1-Q4) that capture different parts of the clock signal (the clock signal is sampled by flip-flops 14-17), the sampling system provides the corresponding indication of frequency for the clock signal based on the plural output signals (Q1-Q4 represent the clock signal H).

As per claim 5, the recited phase detector reads on the phase comparator 2 and the recited phase adjuster is disclosed in column 7, lines 51-55.

As per claim 7, the recited update control reads on the delay line 13 for generating the control signal HE (figure 2). As shown in figure 1, the control signal HE is used to control the frequency of the clock signal H.

As per claim 8, the recited limitation which is the operating characteristics of an integrated circuit chip comprising the system is treated as an intended use of the system because the integrated circuit chip is not further limit the claimed subject matter of claim 1. Accordingly, no patentable weight is given to the recited intended use.

As per claims 10-11, these claims are rejected for the same reason noted in claim 8.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,459,435, issued to Taki.

Taki discloses a system (figure 1), comprising:

a first sampling system (first counter unit 1) that provides an indication of the frequency for a synchronization signal (the signal with the frequency F) received at an input (the node which receives the signal with the frequency F);

a second sampling system (the second counter unit 2) that provides an indication of frequency for an internally generated clock signal (the signal with the frequency F');

a comparator (comparator 4) that provides a comparator signal (the signal from the comparison unit 4 to the data conversion unit 5) based on a comparison of the indication of frequency for the clock signal and the indication of the frequency for the synchronization signal;

a controller (data conversion unit 5 and D/A converter 6) that provides a control signal (the input signal to the VCO 7) for implementing the adjustment to the internally generated clock signal based on the comparator signal;

an oscillator (VCO 7) that adjusts the frequency of the internally generated clock signal based on the control signal.

Taki does not explicitly disclose an update control that controls the sampling rate which controls a rate at which the frequency of the clock signal is updated and the system is packed in an integrated circuit as called for in the claim.

However, Taki discloses that the sampling rate of the system is T (column 4, line 57). He further explicitly discloses the relationship between the sampling rate T and the capability of removing the noise based on the sampling rate which is $1/M*T$ (column 5, lines 60-65). In other words, increasing or decreasing the sampling rate will increase or decrease the ability to remove certain noise components.

It would have been obvious to one skilled in the art at the time of the invention was made to include an update control which can vary the sampling rate T in the system. The motivation and/or suggestion would be to meet the requirement of a certain application which requires the

removing of certain noise components so that the Taki's system can be used in such an application.

Regarding the limitation that the system is packed in an integrated circuit. It is notoriously well-known that a system having elements which are packed in an integrated circuit is more reliable than a system which is built using discreet elements.

It would have been obvious to one skilled in the art at the time of the invention was made to pack all the elements in the Taki's system into an integrated circuit to improve the reliability of the Taki's system.

Response to Arguments

5. Applicant's arguments with respect to the prior art rejections have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

6. Claims 2-4, 6 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-4 are allowable because the prior art of record fails to disclose or suggest the inclusion of the first and second sampling systems wherein the first sampling system samples the frequency of the synchronization signal and the second sampling system, which comprises a delay network, samples the frequency of the clock signal as recited in claim 2.

Claim 6 is allowable because the prior art of record fails to disclose or suggest the inclusion of an insertion loss compensator in the system.

Claim 33 is allowable because the prior art of record fails to disclose or suggest the inclusion of an oscillator/control signal which adjusts the clock signal by switching in or out at least one component in the path of the clock signal.

7. Claim 12 and its dependent claims are allowed for the reason noted in claim 2.
- Claims 18 and 24 and their dependent claims are allowed for the reason noted in claim 6.
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MN
Minh Nguyen
Primary Examiner
Art Unit 2816

10/13/05